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PEARNE & GORDON LLP
1801 EAST 9TH STREET
SUITE 1200
CLEVELAND, OH 44114-3108

EXAMINER	
TRAN, THIEN S	

ART UNIT	PAPER NUMBER
3742	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patdocket@pearne.com
dchervenak@pearne.com

Office Action Summary	**Application No.** 10/599,431	**Applicant(s)** SUENAGA ET AL.
	Examiner THIEN TRAN	**Art Unit** 3742

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/7/2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,13,14 and 16-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13,14 and 16-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/20/2009*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-9, 13, 14 and 16-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Regarding claims 1-3, the claims recite "so that the lowest frequency is set to a first frequency at the beginning of operation of the high-frequency heating apparatus, and the lowest frequency is set to a second frequency which is lower than the first frequency gradually thereafter". The examiner considers this to be indefinite because if the lowest frequency is set as a first frequency, how can the second frequency be set lower than the lowest frequency? If the minimum or lowest frequency is reached then it is not possible to be set at a lower frequency. Appropriate correction is required.

4. Regarding claims 4-9, 13, 14 and 16-31 are also rejected because they are dependent on rejected claims 1, 2 and 3.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3, 13 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Bessyo (US Patent 6,362,463).

7. Regarding claim 1, Bessyo teaches a high-frequency heating apparatus for driving a magnetron (Col 5, Lines 66-67), comprising: a DC power supply (Fig 1, Item 31, Col 7, Line 57) including an AC power supply (Fig 7, AC Source, Col 11, Lines 7-10) a rectifier circuit (Fig 1, Item 40, Col 7, Line 56) for rectifying a voltage of the AC power supply, and a smoothing capacitor (Fig 1, Item 43, Col 9, Lines 55-56) for smoothing an output voltage of the rectifier circuit (Fig 1, Item 35, Col 11, Lines 35-40); a series circuit including two semiconductor switching devices (Fig 1, Items 36 & 37, Col 7, Lines 60-63), the series circuit being connected in parallel to the DC power supply (Fig 1, Items 36 & 37 are connected in parallel to Item 31); a resonance circuit (Fig 1, Items 34 & 35, Col 9, Lines 5-20) connected to a primary winding (Fig 1, Item 33, Col 7, Line 60) of a leakage transformer and a capacitor (Fig 1, Item 32, Col 7, Line 60), one end of the resonance circuit being connected to a middle point of the series circuit (Fig 1, Item 34 is connected between Items 36 and 37) while the other end of the resonance circuit is connected to one end of the DC power supply (Fig 1, Item 34 is connected to positive terminal of Item 31); a drive unit (Fig 1, Item 38, Col 8, Line 20) for driving each of the semiconductor switching devices; a rectifier unit (Fig 1, Item 40, Col 7, Line 56) connected to a secondary winding (Fig 1, Item 39, Col 8, Line 1) of the leakage transformer; a magnetron (Fig 1, Item 41, Col 7, Line 57) connected to the rectifier unit (Fig 1, Item 41 is connected to Item 40); and a dead time generation circuit (Fig 1, Items 34-37) for turning off the semiconductor switching devices concurrently

(Fig 4a & 4c, Items 36 & 37), wherein the drive unit has a function of limiting the lowest frequency of a frequency with which the semiconductor switching devices are driven (Col 13, Lines 5-12), so that the lowest frequency is set to be a first frequency at the beginning of operation of the high-frequency heating apparatus (Fig 13, Col 13, Lines 50-59), and the lowest frequency is set to be a second frequency which is lower that the first frequency gradually thereafter (Col 12, Lines 57-64, Operating frequency is 30 kHz an is then lowered & Col 14, Lines 1-12). Examiner interprets that Bessyo teaches a variable dead time preparation circuit because in Fig 4a & 4c, in modes 2 & 5, the first (Item 36) and second (Item 37) switching devices are simultaneously turned off (Current = 0) in response to the switching frequency.

8. Regarding claim 3, Bessyo teaches a high-frequency heating apparatus for driving a magnetron (Col 5, Lines 66-67), comprising: a DC power supply (Fig 1, Item 31, Col 7, Line 57) including an AC power supply (Fig 7, AC Source, Col 11, Lines 7-10) a rectifier circuit (Fig 1, Item 40, Col 7, Line 56) for rectifying a voltage of the AC power supply, and a smoothing capacitor (Fig 1, Item 43, Col 9, Lines 55-56)for smoothing an output voltage of the rectifier circuit (Fig 1, Item 35, Col 11, Lines 35-40); a series circuit including two semiconductor switching devices (Fig 1, Items 36 & 37, Col 7, Lines 60-63), the series circuit being connected in parallel to the DC power supply (Fig 1, Items 36 & 37 are connected in parallel to Item 31); a resonance circuit (Fig 1, Items 34 & 35, Col 9, Lines 5-20) connected to a primary winding (Fig 1, Item 33, Col 7, Line 60) of a leakage transformer and a capacitor (Fig 1, Item 32, Col 7, Line 60), the resonance circuit being connected in parallel to one of the semiconductor

switching devices (Items 34 & 35 are connected in parallel to Item 37); a drive unit (Fig 1, Item 38, Col 8, Line 20) for driving each of the semiconductor switching devices; a rectifier unit (Fig 1, Item 40, Col 7, Line 56) connected to a secondary winding (Fig 1, Item 39, Col 8, Line 1) of the leakage transformer; a magnetron (Fig 1, Item 41, Col 7, Line 57) connected to the rectifier unit (Fig 1, Item 41 is connected to Item 40); and a dead time generation circuit (Fig 1, Items 34-37) for turning off the semiconductor switching devices concurrently (Fig 4a & 4c, Items 36 & 37), wherein the drive unit has a function of limiting the lowest frequency of a frequency with which the semiconductor switching devices are driven (Col 13, Lines 5-7), so that the lowest frequency is set to a first frequency at the beginning of operation of the high-frequency heating apparatus (Fig 13, Col 13, Lines 50-59), and the lowest frequency is set to a second frequency which is lower frequency gradually thereafter (Col 12, Lines 57-64, Operating frequency is 30 kHz an is then lowered & Col 14, Lines 1-12). Examiner interprets that Bessyo teaches a variable dead time preparation circuit because in Fig 4a & 4c, in modes 2 & 5, the first (Item 36) and second (Item 37) switching devices are simultaneously turned off (Current = 0) in response to the switching frequency.

9. Regarding claims 13 and 30, as applied to claims 1 and 3, Bessyo teaches where the dead time generation circuit (Fig 1, Items 34-37) generates a dead time based on positive and negative offset voltages (Fig 4b & 4d, Items 3 & 37) each varying with a first inclination in proportion to increase of a switching frequency and varying with a second inclination when the switching frequency reaches a predetermined frequency or higher.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 2 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) in view of Manabu (Japan Patent Publication 2003-259643). An English-language equivalent has been adopted for Japanese reference Manabu (Japan Patent Publication 2003-259643) and is included in PTO-892 Notice of Reference Cited.

13. Regarding claim 2, Bessyo teaches a high-frequency heating apparatus for driving a magnetron (Col 5, Lines 66-67), comprising: a DC power supply (Fig 1, Item 31, Col 7, Line 57) including an AC power supply (Fig 7, AC Source, Col 11, Lines 7-10) a rectifier circuit (Fig 1, Item 40, Col 7, Line 56) for rectifying a voltage of the AC power supply, and a smoothing capacitor (Fig 1, Item 43, Col 9, Lines 55-56) for

smoothing an output voltage of the rectifier circuit (Fig 1, Item 35, Col 11, Lines 35-40); a resonance circuit (Fig 1, Items 34 & 35, Col 9, Lines 5-20) connected to a primary winding (Fig 1, Item 33, Col 7, Line 60) of a leakage transformer and a capacitor (Fig 1, Item 32, Col 7, Line 60), a drive unit (Fig 1, Item 38, Col 8, Line 20) for driving each of the semiconductor switching devices; a rectifier unit (Fig 1, Item 40, Col 7, Line 56) connected to a secondary winding (Fig 1, Item 39, Col 8, Line 1) of the leakage transformer; a magnetron (Fig 1, Item 41, Col 7, Line 57) connected to the rectifier unit (Fig 1, Item 41 is connected to Item 40); and a dead time generation circuit (Fig 1, Items 34-37) for turning off the semiconductor switching devices concurrently, wherein the drive unit has a function of limiting the lowest frequency of a frequency with which the semiconductor switching devices are driven (Col 13, Lines 5-7), so that the lowest frequency is set to a first frequency at the beginning of operation of the high-frequency heating apparatus (Fig 13, Col 13, Lines 50-59), and the lowest frequency is set to a second frequency which is lower than the first gradually thereafter (Col 12, Lines 57-64, Operating frequency is 30 kHz an is then lowered & Col 14, Lines 1-12). Examiner interprets that Bessyo teaches a variable dead time preparation circuit because in Fig 4a & 4c, in modes 2 & 5, the first (Item 36) and second (Item 37) switching devices are simultaneously turned off (Current = 0) in response to the switching frequency. Bessyo does not teach two series circuits each including two semiconductor switching devices, each of the series circuits being connected in parallel to the DC power supply; one end of the resonance circuit being connected to a middle point of one of the series circuits

while the other end of the resonance circuit is connected to a middle point of the other series circuit.

14. In analogous art of current resonance type soft switching power circuit, Manabu discloses two series circuits including two semiconductor switching devices (Drawing 1, Q1 & Q2 is the first series circuit, Q3 & Q4 is the second series circuit, Pg 20, Description of Notations), each of the series circuits being connected in parallel to the DC power supply (Drawing 1, First Series (Q1 & Q2) and Second Series (Q3 & Q4) are in parallel with Item E, Pg 20, Description of Notations); one end of the resonance circuit being connected to a middle point of one of the series circuits (Drawing 1, Item 2, Rectification Circuit is connected between Q1 & Q2) while the other end of the resonance circuit is connected to a middle point of the other series circuit (Drawing 1, Item 2, Rectification Circuit is connected between Q2 & Q3) for the benefit of providing soft switching in a current resonance type soft switching power circuit (Abstract, Pg 2, Lines 1-3). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Manabu for the benefit of providing soft switching in a current resonance type soft switching power circuit.

15. Regarding claim 22, as applied to claim 2, Bessyo teaches where the dead time generation circuit (Fig 1, Items 34-37) generates a dead time based on positive and negative offset voltages (Fig 4b & 4d, Items 3 & 37) each varying with a first inclination in proportion to increase of a switching frequency and varying with a second inclination when the switching frequency reaches a predetermined frequency or higher.

16. Claims 4, 5, 6, 24, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) as applied to claims 1 and 3, in view of Noda (US Patent 5,274,208).

17. Regarding claims 4 and 24, Bessyo teaches where frequency of the lowest frequency limiting circuit is set to be higher than the output of the frequency-modulated signal generation circuit at the beginning of operation of the aforementioned high-frequency heating apparatus, and in accordance with time having passed since the beginning of operation, the limited frequency is lowered gradually, while with lowering of the limited frequency, a signal higher in switching frequency of the limited frequency and the output signal of the frequency-modulated signal generation circuit is selected as a signal to be supplied to the dead time generation circuit (Fig 1, Items 34-37) in accordance with time having passed, so that the selected signal is changed over gradually to the output signal of the frequency-modulated signal generation circuit (Fig 15, Item C, Col 14, Lines 20-25 & Col 12, Lines 57-64, Operating frequency is 30 kHz and is then lowered). Bessyo does not teach an error signal generation circuit for generating an error signal from a difference between an input current of the AC power supply and a reference current; and a frequency-modulated signal generation circuit for correcting a rectified voltage/rectified current obtained by rectifying the AC power supply, based on an output (error signal) of the error signal generation circuit, an output of the frequency-modulated signal generation circuit being supplied to the dead time generation circuit; wherein a lowest frequency limiting circuit is inserted between the frequency-modulated signal generation circuit and the dead time generation circuit,

the lowest frequency limiting circuit supplies a limited frequency to the dead time generation circuit based on the output signal of the frequency-modulated signal generation circuit.

18. In analogous art of high frequency heating apparatus, Noda discloses an error signal generation circuit (Fig 2, Item 26, Col 6, Line 44) for generating an error signal from a difference between an input current of the AC power supply and a reference current (Col 6, Lines 39-44); and a frequency-modulated signal generation circuit (Fig 2, Item 27, Col 6, Lines 45-49) for correcting a rectified voltage/rectified current (Fig 2, Item 25, Col 6, Lines 39-42) obtained by rectifying the AC power supply, based on an output (error signal) of the error signal generation circuit, an output of the frequency-modulated signal generation circuit (Fig 2, Item S3, Col 6, Lines 50-54) being supplied to the dead time generation circuit; wherein a lowest frequency limiting circuit (Fig 2, Item 34, Col 7, Lines 13-15) is inserted between the frequency-modulated signal generation circuit and the dead time generation circuit, the lowest frequency limiting circuit supplies a limited frequency (Fig 2, Item S5, Col 7, Line 14-15) to the dead time generation circuit based on the output signal of the frequency-modulated signal generation circuit for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Noda for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied.

19. Regarding claim 5, as applied to claims 1 and 4, Bessyo does not teach where the lowest frequency limiting circuit has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied to the dead time generation circuit, and charges accumulated in the capacitor are discharged. In analogous art of high frequency heating apparatus, Noda discloses where the lowest frequency limiting circuit (Fig 2, Item 34, Col 7, Lines 13-15) has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied (Fig 2, Item Vmax, Col 7, Lines 10-15), to the dead time generation circuit and charges accumulated in the capacitor are discharged (Fig 2, Item S5, Col 7, Lines 12-18) for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Noda for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied. Examiner interprets that it is well known in the art that the overvoltage detection circuit of Noda has a capacitor for generating signal S5 (Fig 2, Item S5, Col 7, Lines 12-18).

20. Regarding claim 6, as applied to claim 1 and 4, the applicant discloses that the dead time generation circuit generates a fixed or marginally increased dead time

regardless of a switching frequency as being well known in the art (Specification, Pg 29, Lines 1-2).

21. Regarding claim 25, as applied to claims 3 and 24, Bessyo does not teach where the lowest frequency limiting circuit has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied to the dead time generation circuit, and charges accumulated in the capacitor are discharged. In analogous art of high frequency heating apparatus, Noda discloses where the lowest frequency limiting circuit (Fig 2, Item 34, Col 7, Lines 13-15) has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied (Fig 2, Item Vmax, Col 7, Lines 10-15), to the dead time generation circuit and charges accumulated in the capacitor are discharged (Fig 2, Item S5, Col 7, Lines 12-18) for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Noda for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied. Examiner interprets that it is well known in the art that the overvoltage detection circuit of Noda has a capacitor for generating signal S5 (Fig 2, Item S5, Col 7, Lines 12-18).

22. Regarding claim 26, as applied to claims 3 and 24, the applicant discloses that the dead time generation circuit generates a fixed or marginally increased dead time regardless of a switching frequency as being well known in the art (Specification, Pg 29, Lines 1-2).

23. Claims 7, 9, 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) as applied to claims 1 and 3, in view of Teruya (Japan Patent Publication 2003-257604). An English-language equivalent has been adopted for Japanese reference Teruya (Japan Patent Publication 2003-257604) and is included in PTO-892 Notice of Reference Cited.

24. Regarding claims 7 and 27, Bessyo does not teach where the dead time generation circuit generates a dead time increased in accordance with increase of a switching frequency. In analogous art of inverter cooker, Teruya discloses where the dead time generation circuit generates a dead time increased in accordance with increase of a switching frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

25. Regarding claim 9, as applied to claims 1 and 7, Bessyo does not teach where the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency. In analogous art of inverter cooker, Teruya discloses where the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

26. Regarding claim 29, Bessyo does not teach where the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency. In analogous art of inverter cooker, Teruya discloses where the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Teruya for the benefit of allowing input to be continuously

variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

27. Claims 8 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) in view of Teruya (Japan Patent Publication 2003-257604) as applied to claims 1, 3 and 7 and further in view of Manabu (Japan Patent Publication 2003-259643). An English-language equivalent has been adopted for Japanese reference Teruya (Japan Patent Publication 2003-257604) and Manabu (Japan Patent Publication 2003-259643) and is included in PTO-892 Notice of Reference Cited.

28. Regarding claim 8, Bessyo in view of Teruya does not teach where the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency. In analogous art of current resonance type soft switching power circuit, Manabu discloses where the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency (Pg 13, 0028, Lines 15-17) for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output (Pg 13, 0028, Lines 16-17). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and Teruya with the disclosure of Manabu for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output.

29. Regarding claim 28, as applied to claims 3 and 27, Bessyo in view of Teruya does not teach where the dead time generation circuit fixes or marginally increases the

dead time at a switching frequency not higher than a predetermined frequency. In analogous art of current resonance type soft switching power circuit, Manabu discloses where the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency (Pg 13, 0028, Lines 15-17) for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output (Pg 13, 0028, Lines 16-17). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and Teruya with the disclosure of Manabu for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output.

30. Claims 14, 18 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) as applied to claims 1 and 3, in view of Yang (US Patent Publication 2005/0174819).

31. Regarding claims 14 and 31, Bessyo teaches where the dead time generation circuit includes a first current varying in proportion to a switching frequency (Fig 4, Item a), a second current beginning flowing at a predetermined frequency at beginning (Fig 13, Col 13, Lines 50-59) and varying in proportion to the switching frequency (Fig 3, Item c). Bessyo does not teach where the dead time generation circuit includes a third current obtaining by and multiplying a combining current of the two currents by a predetermined coefficient, and a upper and lower potential generation unit for generating a set of upper and lower potentials obtained by adding positive and negative offset voltages proportional to the third current, to the duty control power supply respectively, and a dead time is generated based on the set of upper and lower

potentials. In analogous art of synchronous rectification circuit with dead time regulation, Yang discloses where the dead time generation circuit includes a VCC power supply (Pg 2, 0022), a duty control power supply (Pg 2, 0022), a third current obtaining by and multiplying a combining current of the two currents by a predetermined coefficient and a upper and lower potential generation unit for generating a set of upper and lower potentials obtained by adding positive and negative offset voltages proportional to the third current, to the duty control power supply respectively, and a dead time is generated based on the set of upper and lower potentials (Pg 1, 0014) for the benefit of improving the long dead time and efficiency resulting from an unstable voltage waveform (Pg 1, 0012). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Yang for the benefit of improving the long dead time and efficiency resulting from an unstable voltage waveform.

32. Claims 16, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) in view of Manabu (Japan Patent Publication 2003-259643) as applied to claims 2, further in view of Noda (US Patent 5,274,208).

33. Regarding claim 16, Bessyo in view of Manabu teaches where the frequency of the lowest frequency limiting circuit is set to be higher than the output of the frequency-modulated signal generation circuit at the beginning of operation of the aforementioned high-frequency heating apparatus, and in accordance with time having passed since the beginning of operation, the limited frequency is lowered gradually, while with

lowering of the limited frequency, a signal higher in switching frequency of the limited frequency and the output signal of the frequency-modulated signal generation circuit is selected as a signal to be supplied to the dead time generation circuit (Fig 1, Items 34-37) in accordance with time having passed, so that the selected signal is changed over gradually to the output signal of the frequency-modulated signal generation circuit (Fig 15, Item C, Col 14, Lines 20-25 & Col 12, Lines 57-64, Operating frequency is 30 kHz an is then lowered). Bessyo in view of Manabu does not teach an error signal generation circuit for generating an error signal from a difference between an input current of the AC power supply and a reference current; and a frequency-modulated signal generation circuit for correcting a rectified voltage/rectified current obtained by rectifying the AC power supply, based on an output (error signal) of the error signal generation circuit, an output of the frequency-modulated signal generation circuit being supplied to the dead time generation circuit; wherein a lowest frequency limiting circuit is inserted between the frequency-modulated signal generation circuit and the dead time generation circuit, the lowest frequency limiting circuit supplies a limited frequency to the dead time generation circuit based on the output signal of the frequency-modulated signal generation circuit.

34. In analogous art of high frequency heating apparatus, Noda discloses an error signal generation circuit (Fig 2, Item 26, Col 6, Line 44) for generating an error signal from a difference between an input current of the AC power supply and a reference current (Col 6, Lines 39-44); and a frequency-modulated signal generation circuit (Fig 2, Item 27, Col 6, Lines 45-49) for correcting a rectified voltage/rectified current (Fig 2,

Item 25, Col 6, Lines 39-42) obtained by rectifying the AC power supply, based on an output (error signal) of the error signal generation circuit, an output of the frequency-modulated signal generation circuit (Fig 2, Item S3, Col 6, Lines 50-54) being supplied to the dead time generation circuit; wherein a lowest frequency limiting circuit (Fig 2, Item 34, Col 7, Lines 13-15) is inserted between the frequency-modulated signal generation circuit and the dead time generation circuit, the lowest frequency limiting circuit supplies a limited frequency (Fig 2, Item S5, Col 7, Line 14-15) to the dead time generation circuit based on the output signal of the frequency-modulated signal generation circuit for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and Manabu with the disclosure of Noda for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied.

35. Regarding claim 17, Bessyo in view of Manabu does not teach where the lowest frequency limiting circuit has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied to the dead time generation circuit, and charges accumulated in the capacitor are discharged. In analogous art of high frequency heating apparatus, Noda discloses where the lowest frequency limiting circuit (Fig 2, Item 34, Col 7, Lines 13-15) has a capacitor, the

capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied (Fig 2, Item Vmax, Col 7, Lines 10-15), to the dead time generation circuit and charges accumulated in the capacitor are discharged (Fig 2, Item S5, Col 7, Lines 12-18) for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and Manabu with the disclosure of Noda for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied. Examiner interprets that it is well known in the art that the overvoltage detection circuit of Noda has a capacitor for generating signal S5 (Fig 2, Item S5, Col 7, Lines 12-18).

36. Regarding claim 18, the applicant discloses that the dead time generation circuit generates a fixed or marginally increased dead time regardless of a switching frequency as being known in the art (Specification, Pg 29, Lines 1-2).

37. Claims 19, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) in view of Manabu (Japan Patent Publication 2003-259643) as applied to claim 2, further in view of Teruya (Japan Patent Publication 2003-257604).

38. Regarding claim 19, Bessyo in view of Manabu does not teach where the dead time generation circuit generates a dead time increased in accordance with increase of

a switching frequency. In analogous art of inverter cooker, Teruya discloses where the dead time generation circuit generates a dead time increased in accordance with increase of a switching frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and Manabu with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

39. Regarding claim 20, Bessyo does not teach where the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency. In analogous art of current resonance type soft switching power circuit, Manabu discloses where the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency (Pg 13, 0028, Lines 15-17) for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output (Pg 13, 0028, Lines 16-17). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Manabu for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output.

40. Regarding claim 21, Bessyo in view of Manabu does not teach where the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency. In analogous art of inverter cooker, Teruya discloses where the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and Manabu with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

41. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) in view of Manabu (Japan Patent Publication 2003-259643) as applied to claim 2, further in view of Yang (US Patent Publication 2005/0174819).

42. Regarding claim 23, Bessyo in view of Manabu teaches where the dead time generation circuit includes a first current varying in proportion to a switching frequency (Fig 4, Item a), a second current beginning to flow at a predetermined frequency and varying in proportion to the switching frequency (Fig 3, Item c). Bessyo does not teach where the dead time generation circuit includes a third current obtaining by and multiplying a combining current of the two currents by a predetermined coefficient, and a upper and lower potential generation unit for generating two upper and lower

potentials obtained by adding positive and negative offset voltages proportional to the third current, to the duty control power supply respectively, and a dead time is generated based on the two upper and lower potentials. In analogous art of synchronous rectification circuit with dead time regulation, Yang discloses where the dead time generation circuit includes a VCC power supply (Pg 2, 0022), a duty control power supply (Pg 2, 0022), a third current obtaining by and multiplying a combining current of the two currents by a predetermined coefficient and a upper and lower potential generation unit for generating two upper and lower potentials obtained by adding positive and negative offset voltages proportional to the third current, to the duty control power supply respectively, and a dead time is generated based on the two upper and lower potentials (Pg 1, 0014) for the benefit of improving the long dead time and efficiency resulting from an unstable voltage waveform (Pg 1, 0012). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Yang for the benefit of improving the long dead time and efficiency resulting from an unstable voltage waveform.

Response to Amendment

42. Claims 1, 2, 3, 14, 17, 18, 20, 21, 25, 26, 28 and 29 have been amended.

43. Claims 10-12 and 15 have been cancelled.

44. Claims 1-9, 13, 14 and 16-31 are pending.

Response to Arguments

45. Applicant's arguments filed on 12/21/2009 in the Remarks (Pg 13 and 14) with respect to claims 1, 3, 13 and 30 and Bessyo not teaching "the lowest frequency is set to a first frequency at the beginning of operation of the high-frequency heating apparatus, and the lowest frequency is set to a second frequency which is lower than the first frequency gradually thereafter" have been considered but they art not persuasive. The examiner disagrees because Bessyo teaches the lowest frequency is set to a first frequency at the beginning of operation of the high-frequency heating apparatus (Fig 13, Col 13, Lines 50-59), and the lowest frequency is set to a second frequency which is lower than the first frequency gradually thereafter (Col 12, Lines 57-64, Operating frequency is 30 kHz an is then lowered & Col 14, Lines 1-12). The frequency of Bessyo is initially set at about 30 kHz and then if the system of Bessyo is turned off (frequency = 0 kHz) the limitations of the claims are met.

46. The Remarks on page 14 and 15 with respect to claims 2, 20 and 20 and Bessyo in view of Manabu not teaching “the lowest frequency is set to a first frequency at the beginning of operation of the high-frequency heating apparatus, and the lowest frequency is set to a second frequency which is lower than the first frequency gradually thereafter" have been considered but they art not persuasive. The examiner disagrees because Bessyo teaches the lowest frequency is set to a first frequency at the beginning of operation of the high-frequency heating apparatus (Fig 13, Col 13, Lines 50-59), and the lowest frequency is set to a second frequency which is lower than the first frequency gradually thereafter (Col 12, Lines 57-64, Operating frequency is 30 kHz

an is then lowered & Col 14, Lines 1-12). The frequency of Bessyo is initially set at about 30 kHz and then if the system of Bessyo is turned off (frequency = 0 kHz) the limitations of the claims are met.

Conclusion

47. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THIEN TRAN whose telephone number is (571)270-7745. The examiner can normally be reached on Mon-Thurs, 8-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tu Hoang can be reached on 571-272-4780. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/THIEN TRAN/
Examiner, Art Unit 3742
3/24/2010

/TU B HOANG/
Supervisory Patent Examiner, Art Unit 3742